SES's L. S. RAHEJA COLLEGE OF ARTS AND COMMERCE
(AUTONOMOUS)

Syllabus of Digital Electronics & Logic Design LAB under NEP 2020 vertical - VSC with effect from 2024-25

Department of Information Technology and Data Science

HoD/Sr. Person of the Department: Prajakta

Joshi Date of approval by the BoS: 27/04/4024

Approved by the Academic Council: 29/04/2024

Ratified by the Governing Body on: 06/05/2024

Programme: B.Sc.(IT)				Semester : I	
Course : Digital Electronics & Logic Design LAB Academic Year: 2024-2025 Batch: 2024-2027				Code: UGBSCITIVSC224	
Teaching Scheme			Evaluation Scheme		
Lectures	Practical	Tutorials	Credits	Internal Continuous Assessment (ICA) (weightage)	Term End Examinations (TEE) (weightage)
Nil	30	Nil	1	-	25

Learning Objectives :	1. To apply and test the gates learnt using various IC's. 2. To evaluate the Boolean expression to reduce and minimize the gates used
Learning Outcomes :	1. Construct basic and universal logic circuits. 2. Verify the functionalities of various IC's. 3. Design circuits using K-maps minimization technique 4. Design and test Encoders, Decoders, Multiplexers and Demultiplexers
Pedagogy:	Experiential learning, logic building, practical implementation

Detailed Syllabus: (per session plan)
Session Outline For: Digital Electronics & Logic Design LAB
Each lecture session would be of one hour duration (30 sessions).

Practical	Content	Practical Wise Pedagogy Used	Practical Wise Duration
I	Study of basic gates and Universal gates	logic building, practical implementation with hardware kit	6
II	Study of Boolean expressions	logic building, practical implementation with hardware kit	6
III	Design a Combinational Circuits using K- maps	logic building, practical implementation with hardware kit	6
IV	Implement Adder and Subtractor circuits	logic building, practical implementation with hardware kit	6
V	Design Multiplexers and Demultiplexers	logic building, practical implementation with hardware kit	6